

# KARA-A2

# Product SPEC

Version: 0.5

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## 1. Introduction

### 1.1 Overview

KARA-A2 is a 3D sensing module, with 2 IR cameras and 1 RGB camera. The main SOC is Altek's AL6100 which is a high resolution real-time depth chip for 3D applications.

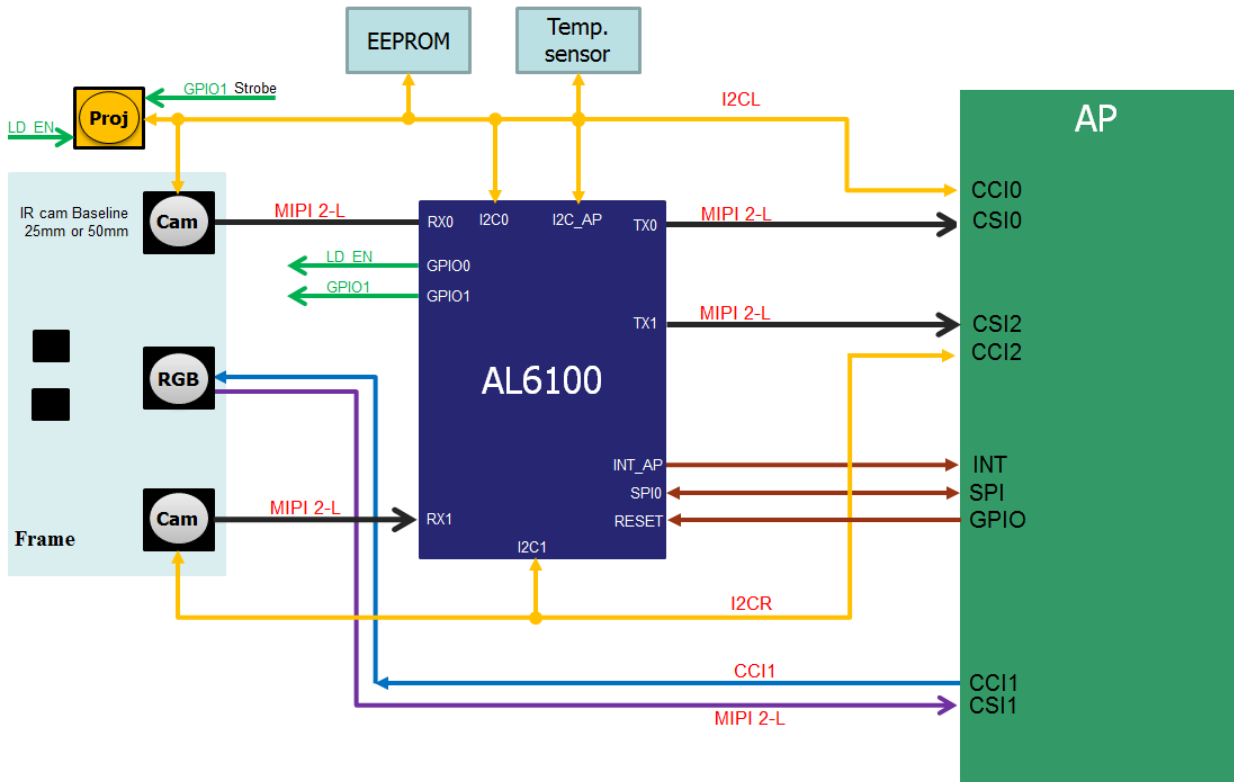
### 1.2 Features

- IR camera: OV09282-GA4A
  - Resolution: 1280x800
  - Type: Fixed Focus(FF)
  - Image size: 1280x720, 640x480, 640x400
  - I2C slave address: 0x60(7-bit, ID pulled low)
- RGB camera: OV13855
  - Resolution: 4224x3136
  - Type: Auto Focus(AF)
  - Image size: 4224x3136, 4224x2376, 2112x1568, and more
  - I2C slave address: 0x10(7-bit, see the module spec for detailed)
- Depth chip: AL6100
  - Depth map output, resolution up to 720p/30fps@10-bit depth map and 3-bit confidence map.
  - Resolution: up to 1280x720@16:9 / 960x720@4:3
- EEPROM: GT24C512B-2UDLI\_TR
  - 512kbit for dual-cam calibration data
  - I2C slave address: 0x51(7-bit)
- Temperature sensor: CAT34TS00VP2GT4A
  - Digital temperature sensor 1.8V
  - Range: -20°C to +125°C
  - Resolution: 12 bits
  - I2C slave address: 0x19(7-bit)
- LD driver: ADP1660
  - 2-ch LD flash driver
  - Up to 750mA per channel
  - I2C slave address: 0x30(7-bit)

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- Dot projector: Belice, Type-A x1 & Type-B x1
    - Type-A with 5° pattern rotation, Type-B with 15° pattern rotation
    - Number of dots: 10,000@80° field of illumination(pair of emitters)
    - Default: 387mA(adjustable, 0~387mA)
  - Module connector: DF40C(2.0)-60DS-0.4V(51)
    - 60 pins board to board connector
    - Pitch 0.4mm
  - Operating temperature: 0°C ~+50°C

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### 1.3 System block diagram



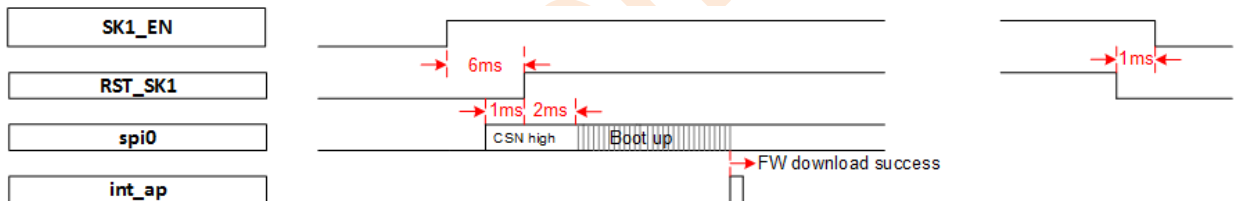
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## 1.4 Connectivity

- MIPI interface
  - MIPI D-PHY TX
    - ◆ D-PHY can be configured to 1 or 2-lane, up to 2.5Gbps
  - MIPI CSI-2 v1.2
- I2C interfaces, x3
  - For 3 cameras control
  - I2C0(SDA/SCL\_RX0) and I2C1(SDA/SCL\_RX1) are also connected to AL6100
- 4-wire SPI interface
  - Up to 50MHz, slave mode. Boot from host's SPI.

## 2. Power On-Off Sequence



Note1: PWR can be always on.

Note2: int\_ap is AL6100's output signal.

Note3: Equation for SPI boot up frequency limitation(boot code loading):

$$\text{SPI\_CLK freq. (max)} = \text{MCLK(6~27MHz)} * 0.65$$

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### 3. Signal Descriptions

#### 3.1 Pin List

##### SPI

Pin Name	Pin Number	I/O	Internal Pull	Description
spi0_csn	49	I	I-up	SPI0 chip select
spi0_clk	47	I	I-down	SPI0 clock
spi0_do	45	O	I-down	SPI0 data output
spi0_di	43	I	I-up	SPI0 data input

##### I2C

Pin Name	Pin Number	I/O	Internal Pull	Description
SCL_RX0	8	I/O	I-up	connected to IR-Left, EEPROM, Temperature sensor, LD driver and AL6100's I2C0 & I2C_AP
SDA_RX0	10	I/O	I-up	connected to IR-Left, EEPROM, Temperature sensor, LD driver and AL6100's I2C0 & I2C_AP
SCL_RX1	26	I/O	I-up	connected to IR-Right and AL6100's I2C1
SDA_RX1	28	I/O	I-up	connected to IR-Right and AL6100's I2C1
SCL_CSI1	48	I	I-up	connected to RGB-cam
SDA_CSI1	50	I/O	I-up	connected to RGB-cam

##### Clock

Pin Name	Pin Number	I/O	Internal Pull	Description
CAM_CLK0	12	--	--	reserved(NC)
MCLKOUT_CSI1	42	--	--	reserved(NC)

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## I/O pins

Pin Name	Pin Number	I/O	Internal Pull	Description
RST_SK1	53	I	I-up	AL6100 reset input, 2k resistor pull up
int_ap	51	O	I-down	AL6100 interrupt output
EEWP	11	I	I-up	EEPROM write protect, 2k resistor pull up
PWDN_360	14	--	--	reserved(NC)
FSIN0	16	I/O	--	frame sync pin connection, connected the 3 cameras
XVS_CSI1	46	I/O	--	default: connected to FSIN0
RSTN_CSI1	44	I	--	RGB camera reset pin, active low
SK1_EN	60	I	--	KARA-A2 module power enable

## MIPI interface

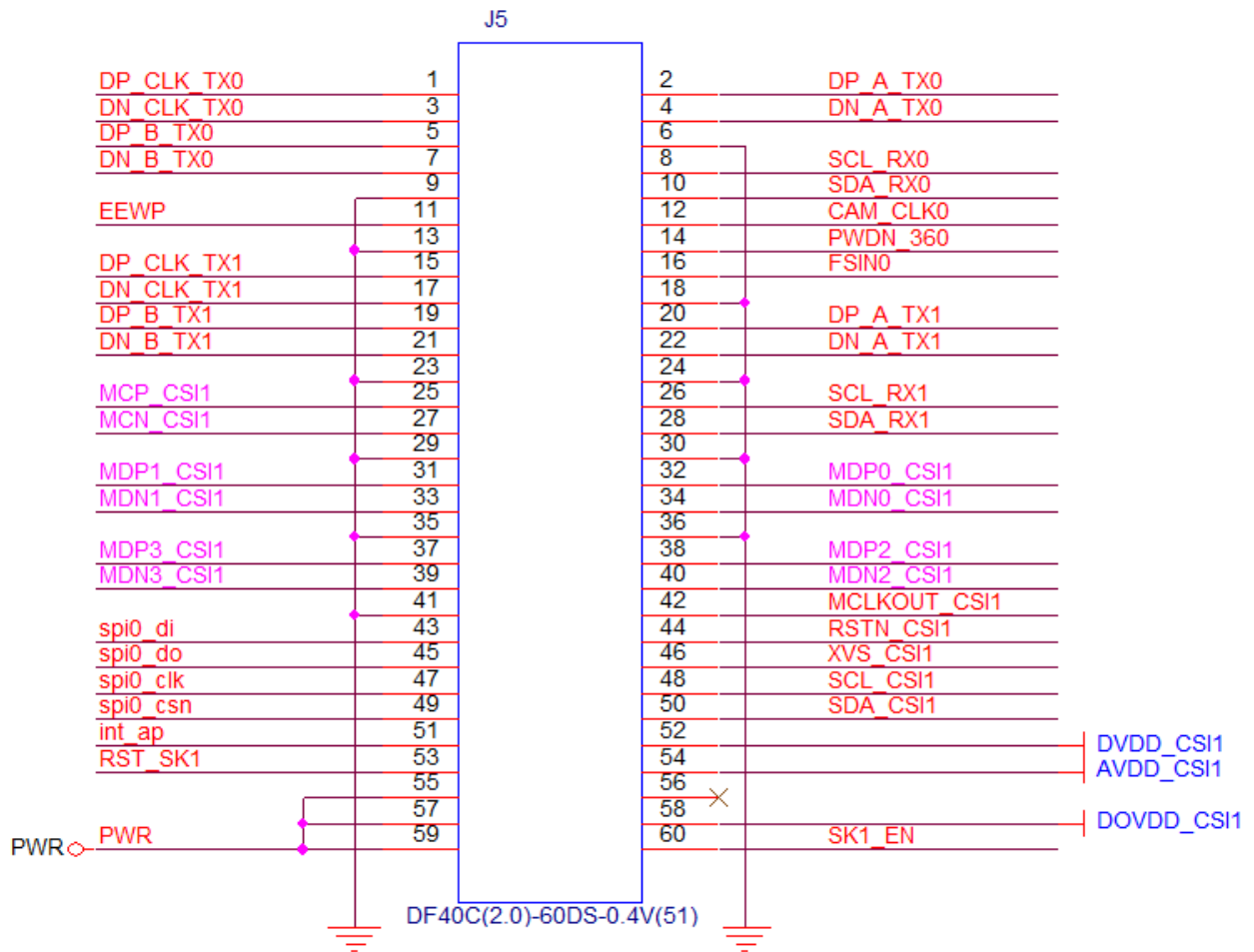


Pin Name	Pin Number	I/O	Internal Pull	Description
DP_A_TX0 DN_A_TX0	2 4	No	--	AL6100 MIPI TX0 lane 0
DP_B_TX0 DN_B_TX0	5 7	No	--	AL6100 MIPI TX0 lane 1
DP_CLK_TX0 DN_CLK_TX0	1 3	No	--	AL6100 MIPI TX0 clock lane
DP_A_TX1 DN_A_TX1	20 22	No	--	AL6100 MIPI TX1 lane 0
DP_B_TX1 DN_B_TX1	19 21	No	--	AL6100 MIPI TX1 lane 1
DP_CLK_TX1 DN_CLK_TX1	15 17	No	--	AL6100 MIPI TX1 clock lane
MDP0_CSI1 MDN0_CSI1	32 34	No	--	RGB-cam MIPI lane 0
MDP1_CSI1 MDN1_CSI1	31 33	No	--	RGB-cam MIPI lane 1
MDP2_CSI1 MDN2_CSI1	38 40	No	--	RGB-cam MIPI lane 2
MDP3_CSI1 MDN3_CSI1	37 39	No	--	RGB-cam MIPI lane 3
MCP_CSI1 MCN_CSI1	25 27	No	--	RGB-cam MIPI clock lane

### Power & GND

Pin Name	Pin Number	Description
PWR	55,57,59	KARA-A2 module power
GND	6,9,13,18,23,24,29,30,35,36,41,	KARA-A2 module ground
DVDD_CSI1	52	RGB VDD, 1.2V input
AVDD_CSI1	54	RGB AVDD, 2.8V input
DOVDD_CSI1	58	RGB IOVDD, 1.8V input
(NC)	56	reserved

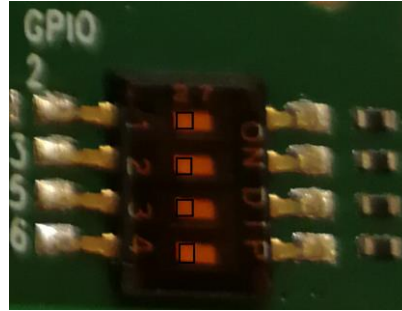
## 3.2 Module Connector



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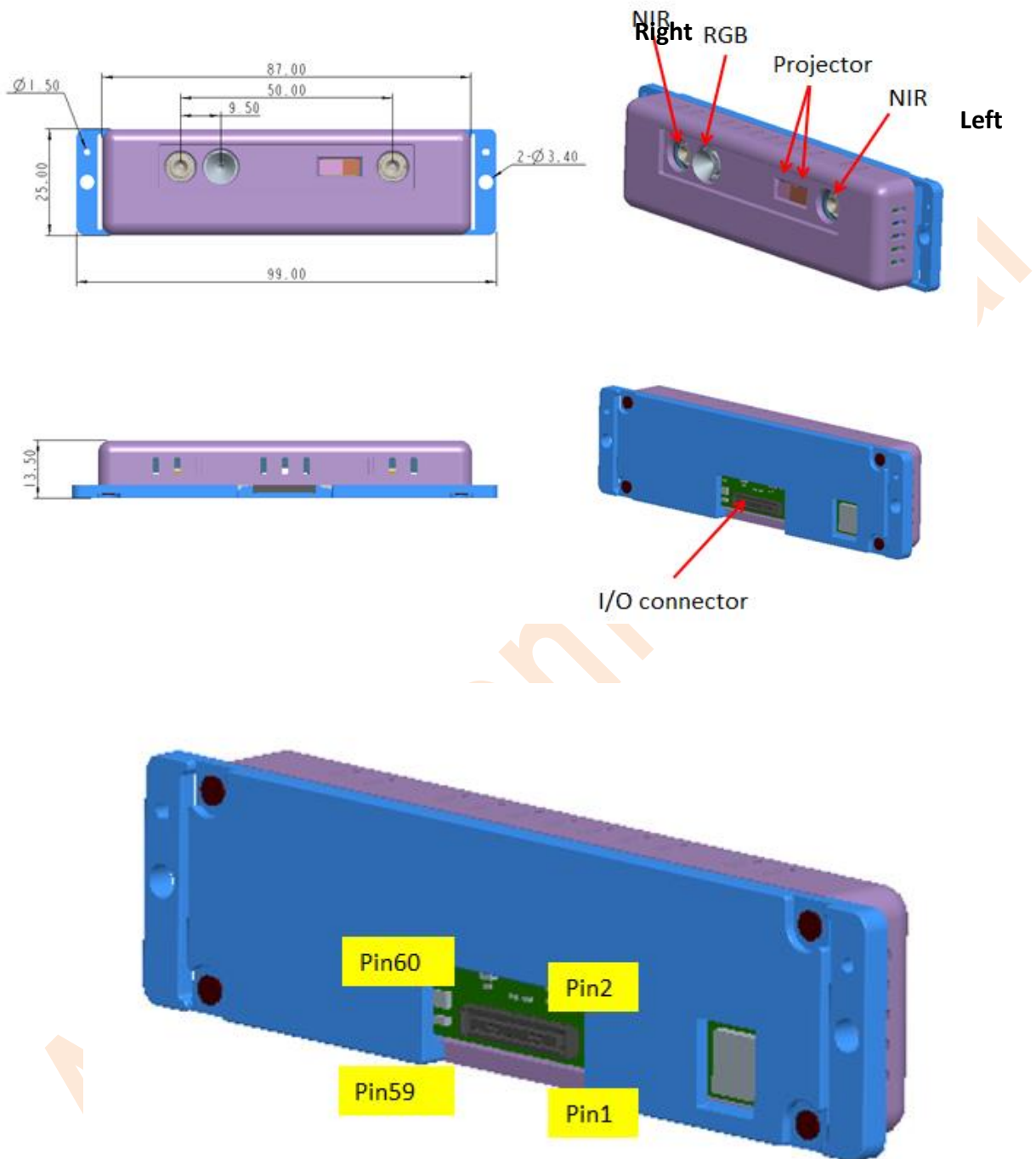
### 3.3 Bootstrap Settings

- There're 4 pins used as AL6100 bootstrap settings, GPIO\_2,3,5,6.
- It's for engineering usage only, keep the switch on the left-side for normal applications.



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## 4. Module outline and definition



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## 5. Electrical Specifications

### 5.1 Absolute maximum ratings

**Table 5.1: Absolute maximum ratings**

Symbol	Parameter	Value(max)	Unit
PWR	Module power supply	5.5	V
DVDD_CSI1	RGB DVDD	3.0	V
AVDD_CSI1	RGB AVDD	4.5	V
DOVDD_CSI1	RGB VDDIO	4.5	V

### 5.2 Recommended operating conditions

**Table 5.2: Recommended operating conditions**

Symbol	Min	Typical	Max
PWR	3.5V	4.0V	5.0V
DVDD_CSI1	1.14V	1.2V	1.26V
AVDD_CSI1	2.7V	2.8V	3.0V
DOVDD_CSI1	1.7V	1.8V	1.9V

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## 5.3 DC characteristic

**Table 5.3: DC Characteristic**

Symbol	Parameter	Min.	Typ.	Max.	Unit
V <sub>IL</sub>	I/O Input low	-	-	0.5	V
V <sub>IH</sub>	I/O Input high	0.75*VDDI 0	-	-	V
V <sub>OL</sub> (*1)	I/O Output low	-	-	0.4	V
V <sub>OH</sub> (*2)	I/O Output high	0.75*VDDI 0		VDDIO	V
I <sub>dd</sub>	PWR operating current		350(*3)		mA
I <sub>dd-A</sub>	AVDD_CSI1 operating current		36		mA
I <sub>vddio</sub>	DOVDD_CSI1 operating current		3		mA
I <sub>dd-d</sub>	DVDD_CSI1 operating current		106(*4)		mA

\*1: test condition I<sub>OL</sub> < 2mA

\*2: test condition I<sub>OH</sub> < 2mA

\*3: This is average current consumption on typical application. It will depend on system test conditions, especially the exposure time duration. Please not the peak current could be about 1.5A@4.0V

\*4: Check with the RGB sensor specification for detailed DC characteristic.

## 6. SPI Timing Specification

**Table 6.1: Four-Wire SPI Slave**

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
fSCLK	Serial interface input clock	-			50	MHz
Clock duty	-	-	45	50	55	%
tCSS	CS setup time	Slave input	10			ns
tCSH	CS hold time	Slave input	10			ns
tDSU	Data setup time	Slave input	3			ns
tDH	Data hold time	Slave input	3			ns
tDOH	Data output hold time	Slave output	0			ns
tDOV	Data output valid time	Slave output (under Cload=15pF)			7.5	ns
tDIS	Data output disable time	Slave output			7.5	ns

\*1: T is fSCLK clock cycle time.

**Figure 6.1: SPI Timing Diagram**

